

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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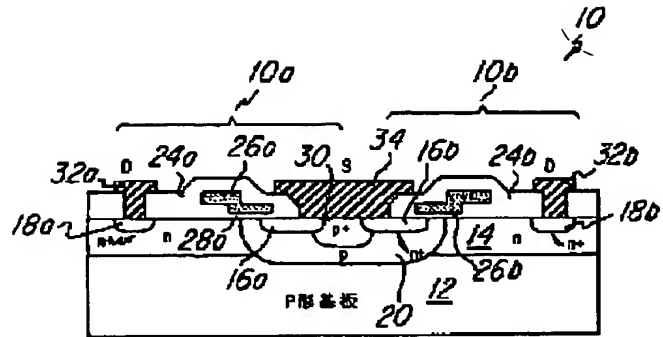
APPLICATION DATE : 01-07-94  
APPLICATION NUMBER : 06151351

APPLICANT : TEXAS INSTR INC <TI>;

INVENTOR : OU KYONG KUUON;

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TITLE : MANUFACTURE OF SELF-ALIGNED  
HORIZONTAL DMOS TRANSISTOR



ABSTRACT : PURPOSE: To provide a manufacturing method for a self-aligned horizontal DMOS transistor, which has the best ON-resistance characteristic and breakdown voltage, has the simple constitution and can be applied to many fields.

CONSTITUTION: An insulating layer 24, such as field oxide is, formed on a semiconductor layer 14. Then, in order to expose a source window and a drain window, the insulating layer is patterned. Then, a D-well region 20 is formed in the source-window part of the semiconductor layer. A sidewall region is formed at the neighborhood of the sidewall of the insulating layer around the source window. Then, source regions 16 and drain regions 18 are formed by, for example, implanting ions. Gate electrodes 26 are formed on a part of the D-well region 20 between the source region and the insulating layer and on the channel region in the D-well between the source and the drain.

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